



Advanced
Micro
Devices

Am9128

2048x8 Static RAM

DISTINCTIVE CHARACTERISTICS

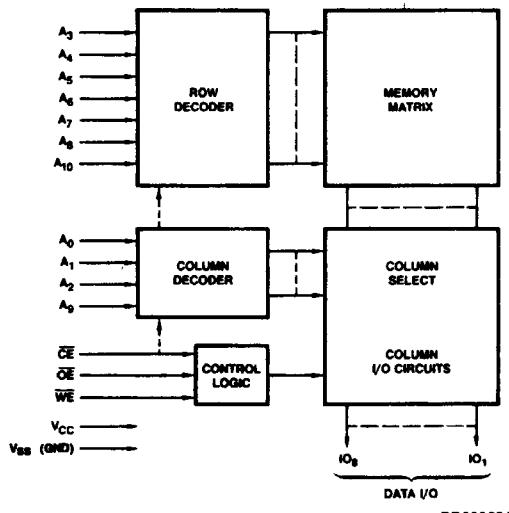
- Logic voltage levels compatible with TTL
- Three-state output buffers and common I/O
- I_{CC} Max., as low as 100 mA
- t_{AA}/t_{ACs} as low as 70 ns
- Power-Down mode (I_{SB} as low as 15 mA)

GENERAL DESCRIPTION

The Am9128 is a 16,384-bit Static Random Access Memory organized as 2048 words of 8 bits. It uses fully static circuitry, requiring no clocks or refresh to operate. Directly TTL-compatible inputs and outputs and operation from a single +5 V supply simplify system

designs. Common data I/O pins using three-state outputs are provided. The Am9128 is available in an industry-standard 24-pin DIP package with 0.6-inch pin row spacing. The Am9128 uses the JEDEC standard pinout for byte-wide memories (compatible to 16K EPROMs).

BLOCK DIAGRAM



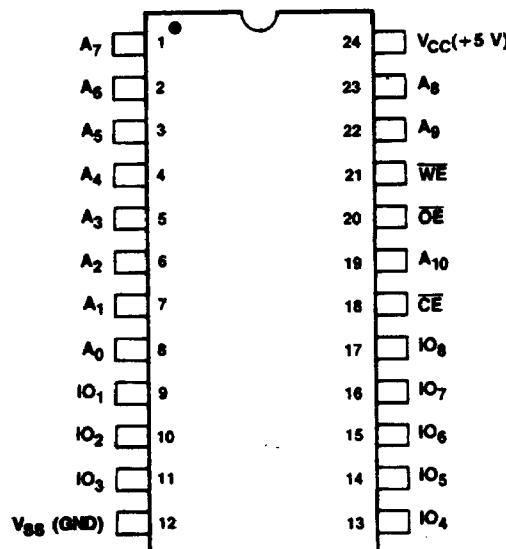
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PRODUCT SELECTOR GUIDE

Part Number	Am9128-70	Am9128-90	Am9128-10	Am9128-12	Am9128-15	Am9128-20
Maximum Access Time (ns)	70	90	100	120	150	200
Maximum Operating Current (mA)	0 to 70°C	140	N/A	120	N/A	100
	-55° to 125°C	N/A	180	N/A	150	150
Maximum Standby Current (mA)	0° to 70°C	30	N/A	15	N/A	15
	-55° to 125°C	N/A	30	N/A	30	30

CONNECTION DIAGRAMS
Top View

DIPs



CD000121

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

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Address Designators	
External	Internal
A ₃	AX ₀
A ₄	AX ₁
A ₅	AX ₂
A ₆	AX ₃
A ₇	AX ₄
A ₈	AX ₅
A ₁₀	AX ₆
A ₀	AY ₀
A ₁	AY ₁
A ₂	AY ₂
A ₉	AY ₃



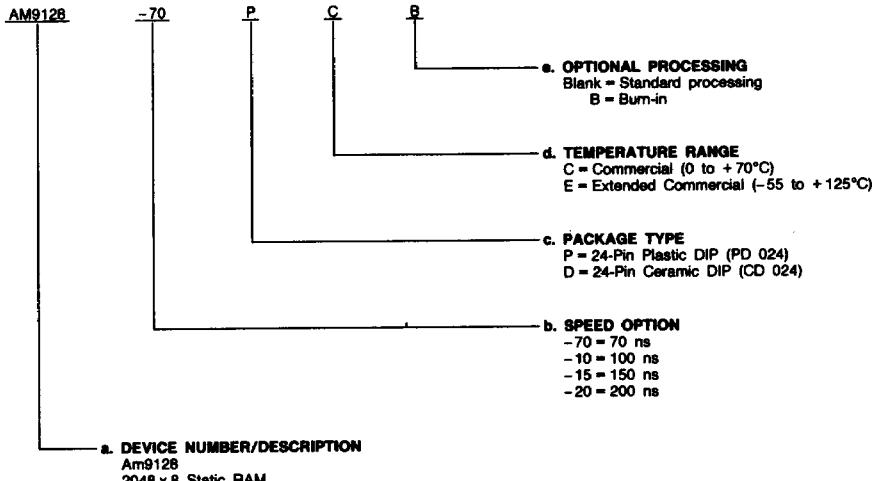
DIE SIZE: 0.162" x 0.240"

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM9128-70	PC, DC, DCB, DE, DEB
AM9128-10	
AM9128-15	
AM9128-20	

Valid Combinations

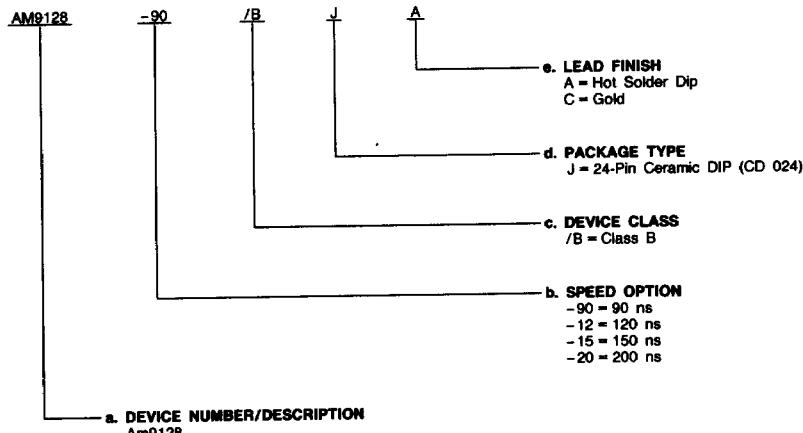
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



a. DEVICE NUMBER/DESCRIPTION

AM9128
2048 x 8 Static RAM

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
AM9128-90	
AM9128-12	/BJA, /BJC
AM9128-15	
AM9128-20	

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11

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PIN DESCRIPTION

A₀ - A₁₀ Addresses (Input)

The 10-bit field presented at the address inputs selects one of the 2048 memory locations to be read from — or written into — via the data lines.

I/O₁ - I/O₈ Data In/Out Port (Input/Output)

If WE is LOW, the data represented on the I/O lines can be written into the selected memory location. If WE is HIGH, the I/O lines represent the data read from the selected memory location.

CE Chip Enable (Input, Active LOW)

Read and Write cycles can be executed only when CE is LOW.

WE Write Enable (Input, Active LOW)

Data is written into the memory if WE is LOW and read from the memory if WE is HIGH.

OE Output Enable (Input, Active LOW)

Read cycles can be executed only when OE is LOW.

ABSOLUTE MAXIMUM RATINGS (Note 11)

Storage Temperature	-65 to +150°C
Ambient Temperature with Power Applied	-55 to +125°C
Supply Voltage	-0.5 V to +7.0 V
Signal Voltage with Respect to Ground	-3.0 V to +7.0 V
Power Dissipation	1.0 W
DC Output Current	10 mA

*Maximum ratings are to be for system design reference, parameters given may not be 100% tested by AMD.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted) (Note 3)

Parameter Symbol	Parameter Description	Test Conditions		Am9128-90		Am9128-10		Am9128-15		Am9128-70		Am9128-12		Am9128-20		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I _{OH}	Output HIGH Current	V _{OH} = 2.4 V	V _{CC} = 4.5 V	-2		-2		-2		-2		-2		-2		mA
I _{OL}	Output LOW Current	V _{OL} = 0.4 V		4		4		4		4		4		4		mA
V _{IH}	Input HIGH Voltage			2.0	V _{CC} + 1.0	2.0	V _{CC} + 1.0	2.0	V _{CC} + 1.0	2.0	V _{CC} + 1.0	2.0	V _{CC} + 1.0	2.0	V _{CC} + 1.0	V
V _{IL}	Input LOW Voltage			-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	V _{SS} ≤ V _I ≤ V _{CC}			10		10		10		10		10		10	μA
I _{OZ}	Output Leakage Current	V _{SS} ≤ V _O ≤ V _{CC} Output Disabled			10		10		10		10		10		10	μA
C _{IN}	Input Capacitance (Note 12)	Test Frequency = 1.0 MHz, T _A = 25°C, All pins at 0	V _{CC} = 5.0 V		6		6		6		6		6		6	pF
C _{I/O}	Input/Output Capacitance (Note 12)				7		7		7		7		7		7	pF
I _{CC}	V _{CC} Operating Supply Current	Max. V _{CC} , CE ≤ V _{IL} Outputs Open	COM'L	120		100		140								mA
				MIL-E-COM'L	180		150		150		150		150		150	
I _{SB}	Automatic CE Power Down Current	Max. V _{CC} , CE ≥ V _{IH}	COM'L	15		15		30								mA
				MIL-E-COM'L	30		30		30		30		30		30	
I _{PO}	Peak Power On Current (Note 12)	V _{CC} = GND to V _{CC} Max. CE ≥ V _{IH} (Note 2)	COM'L	15		15		30								mA
		MIL-E-COM'L		30		30		30		30		30		30		

- Notes:
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
 - A pull up resistor to V_{CC} on the CE input is required during power up to keep the device deselected, otherwise I_{PO} will exceed values given.
 - For test and correlation purposes, ambient temperature is defined as the "instant-on" case temperature.
 - At any given temperature and voltage condition, t_{HZ} is less than t_{LZ}.
 - WE is HIGH for read cycle.
 - Device is continuously selected, CE = V_{IL}.
 - Address valid prior to or coincident with CE transition LOW.
 - OE = V_{IL}.
 - C_L = 30 pF.
 - Transition is measured from 1.5 V on the input to V_{OH} - 500 mV and V_{OL} + 500 mV on the outputs using the load shown in Switching Test Circuits. C_L = 5 pF.
 - The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling, and use to avoid exposure to excessive voltages.
 - The parameter is guaranteed by characterization, but is not tested.

OPERATING RANGES (Note 3)

Commercial (C) Devices	Ambient Temperature (T _A)	0 to +70°C
	Supply Voltage (V _{CC})	+4.5 V to +5.5 V
Military* (M) and Extended Commercial (E) Devices	Case Temperature (T _A)	-55 to +125°C
	Supply Voltage (V _{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products,
Group A, Subgroups 9, 10, 11 are tested unless otherwise noted.)

Am9128-70, -90, -10

No.	Parameter Symbol	Parameter Description	Am9128-70		Am9128-90		Am9128-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
1	t _{RC}	Read Cycle Time	70		90		100		ns
2	t _{ACC}	Address Access Time (Note 9)		70		90		100	ns
3	t _{ACS}	Chip Select Access Time (Note 9)		70		90		100	ns
4	t _{OE}	Output Enable Time	COM'L	40		N/A		50	ns
		(Note 9)	MIL		N/A	50		N/A	
5	t _{OH}	Output Hold Time from Address Change	5		5		5		ns
6	t _{CLZ}	Output in Low-Z from CE (Notes 4, 10, 12)	5		5		5		ns
7	t _{CHZ}	Output in Hi-Z from CE (Notes 4, 10, 12)		35		40		40	ns
8	t _{OLZ}	Output in Low-Z from OE (Notes 4, 10, 12)	5		5		5		ns
9	t _{OHZ}	Output in Hi-Z from OE (Notes 4, 10, 12)		30		35		35	ns
10	t _{Pu}	Chip Selection to Power-Up Time (Note 12)	0		0		0		ns
11	t _D	Chip Deselection to Power-Down Time (Note 12)		40		45		50	ns
WRITE CYCLE									
12	t _{WC}	Write Cycle Time	70		90		100		ns
13	t _{CW}	Chip Selection to End of Write (Note 1)	0 to +70°C -55 to -125°C	60 N/A		N/A 80		90 N/A	ns
14	t _{AS}	Address Setup Time	5		10		10		ns
15	t _{WP}	Write Pulse Width (Note 1)	40		55		60		ns
16	t _{WR}	Write Recovery Time	5		5		5		ns
17	t _{DS}	Data Setup Time	30		35		40		ns
18	t _{DH}	Data Hold Time	5		5		5		ns
19	t _{WLZ}	Output in Low-Z from WE (Notes 4, 10, 12)	5		5		5		ns
20	t _{WHZ}	Output in Hi-Z from WE (Notes 4, 10, 12)		30		35		35	ns
21	t _{AW}	Address to End of Write	65		80		80		ns

Notes: See notes following DC Characteristics table.

SWITCHING CHARACTERISTICS (Cont'd.)

Am9128-12, -15, -20

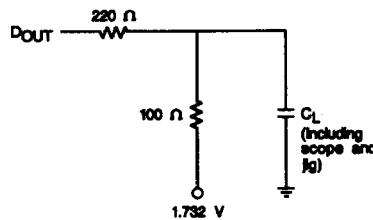
No.	Parameter Symbol	Parameter Description	Am9128-12		Am9128-15		Am9128-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
1	t_{RC}	Read Cycle Time	120		150		200		ns
2	t_{ACC}	Address Access Time (Note 9)		120		150		200	ns
3	t_{ACS}	Chip Select Access Time (Note 9)		120		150		200	ns
4	t_{OE}	Output Enable Time (Note 9)	COM'L		N/A	60		70	ns
			MIL		70	70		80	
5	t_{OH}	Output Hold Time from Address Change	5		5		5		ns
6	t_{CLZ}	Output in Low-Z from CE (Notes 4, 10, 12)	5		5		5		ns
7	t_{CHZ}	Output in Hi-Z from CE (Notes 4, 10, 12)		50		55		55	ns
8	t_{CLZ}	Output in Low-Z from OE (Notes 4, 10, 12)	5		5		5		ns
9	t_{CHZ}	Output in Hi-Z from OE (Notes 4, 10, 12)		45		50		50	ns
10	t_{PU}	Chip Selection to Power-Up Time (Note 12)	0		0		0		ns
11	t_{PD}	Chip Deselection to Power-Down Time (Note 12)		55		60		60	ns
WRITE CYCLE									
12	t_{WC}	Write Cycle Time	120		150		200		ns
13	t_{CW}	Chip Selection to End of Write (Note 1)	COM'L		N/A	120		150	ns
			MIL		105	130		160	
14	t_{AS}	Address Setup Time	10		20		20		ns
15	t_{WP}	Write Pulse Width (Note 1)	70		85		100		ns
16	t_{WR}	Write Recovery Time	5		5		5		ns
17	t_{DS}	Data Setup Time	45		50		60		ns
18	t_{DH}	Data Hold Time	5		5		5		ns
19	t_{WLZ}	Output in Low-Z from WE (Notes 4, 10, 12)	5		5		5		ns
20	t_{WHZ}	Output in Hi-Z from WE (Notes 4, 10, 12)		50		50		50	ns
21	t_{AW}	Address to End of Write	105		120		120		ns

Notes: See notes following DC Characteristics table.

SWITCHING TEST CONDITIONS

Input Pulse Levels	.4 to 2.4 V
Input Rise and Fall Times	10 ns
Input Timing Reference Levels	1.4 V
Output Timing Reference Levels	1.4 V

SWITCHING TEST CIRCUIT



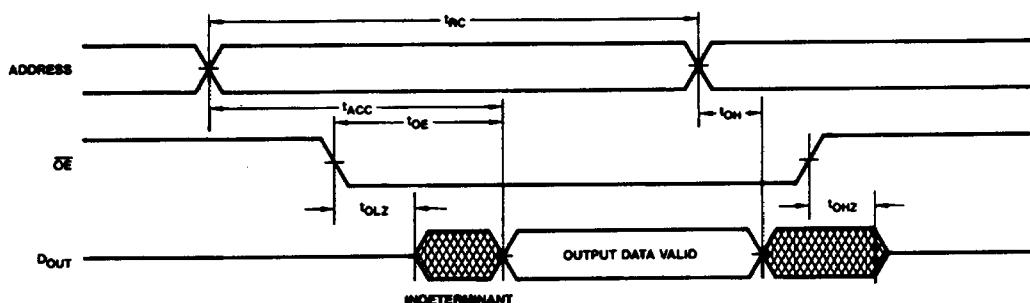
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SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

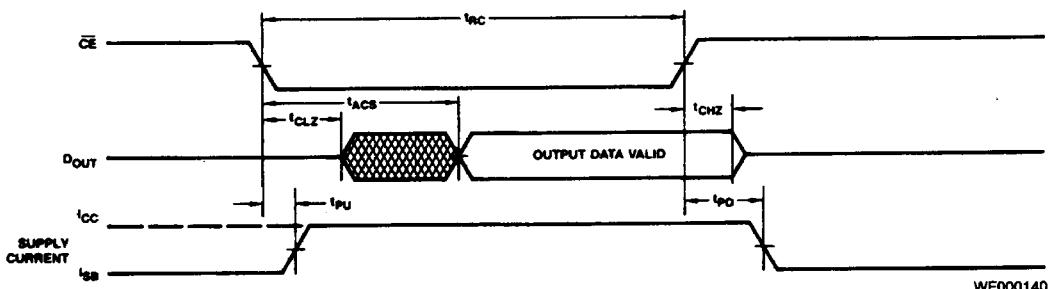
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE 'OFF' STATE

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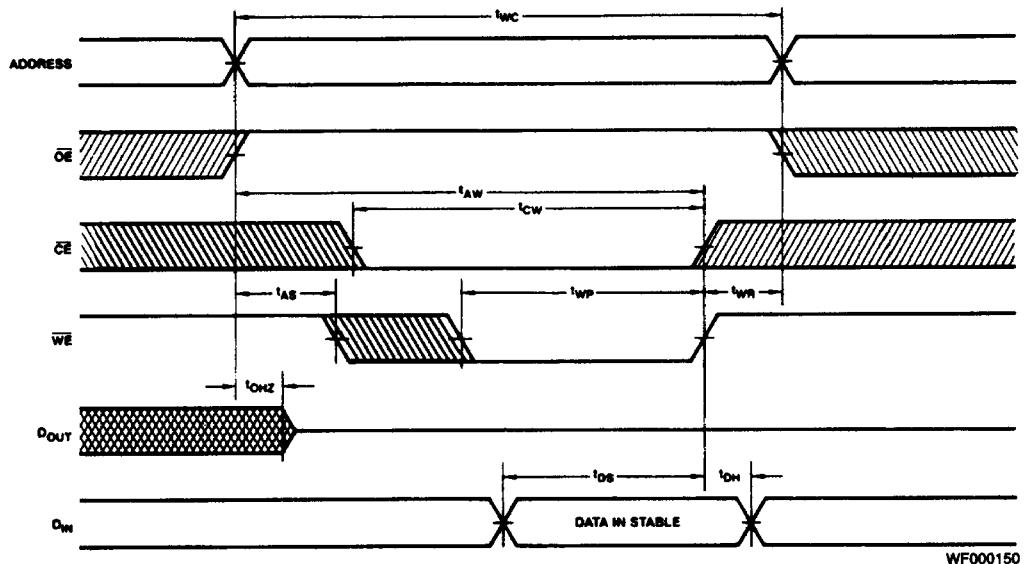
Read Cycle No. 1 (Notes 5, 6)



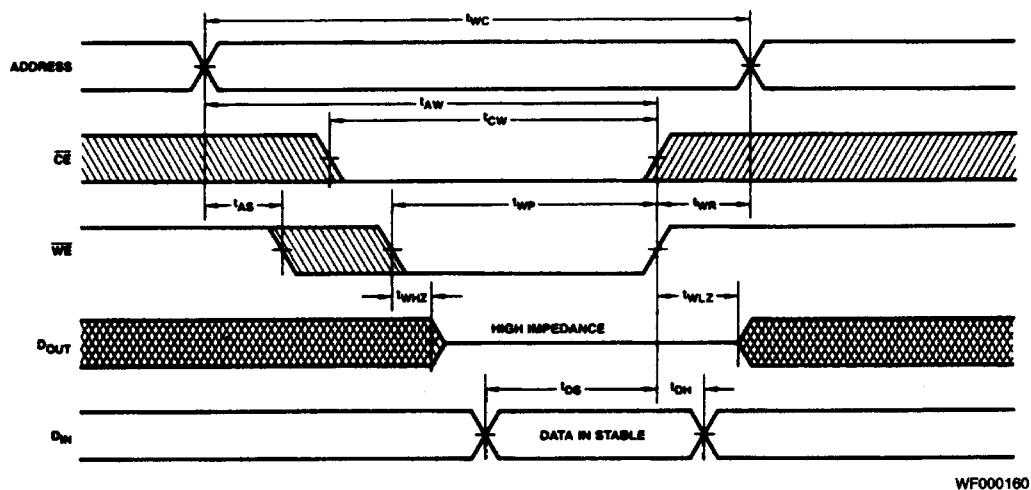
Read Cycle No. 2 (Notes 5, 7, 8)

Notes: See notes following DC Characteristics table.

SWITCHING WAVEFORMS (Cont'd.)



Write Cycle No. 1

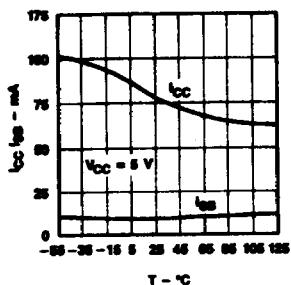


Write Cycle No. 2 (Notes 7, 8)

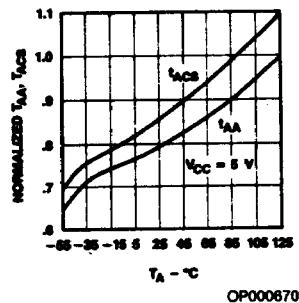
Notes: See notes following DC Characteristics table.

TYPICAL PERFORMANCE CURVES

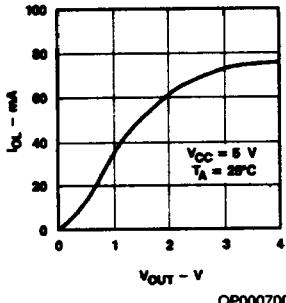
**Supply Current
Versus Ambient Temperature**



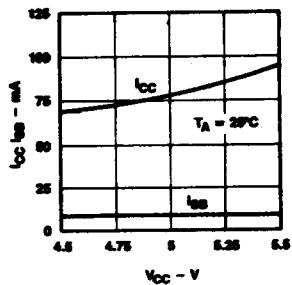
**Normalized Access Time
Versus Ambient Temperature**



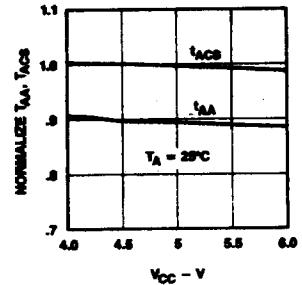
**Output Sink Current
Versus Output Voltage**



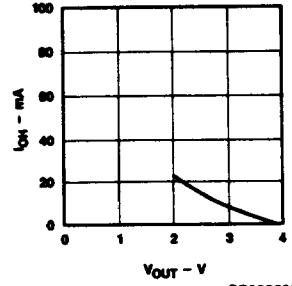
**Supply Current
Versus Supply Voltage**



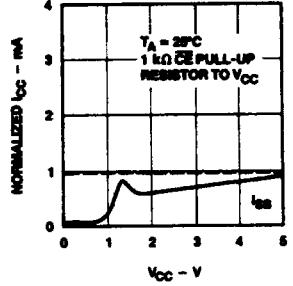
**Normalized Access Time
Versus Supply Voltage**



**Output Source Current
Versus Output Voltage**



**Typical Power-On Current
Versus Power Supply**



**Access Time Change
Versus Input Voltage**

